What Is Claimed Is:

1. A receiver circuit for outputting signals to an internal circuit supplied with a first power supply voltage, comprising:

a reference voltage circuit supplied with the first power supply voltage for outputting a reference voltage that is a mid-point voltage between the first power supply voltage and ground;

a reference current circuit for generating a first current according to the reference voltage; and

a receiving circuit supplied with a second power supply voltage higher than the first power supply voltage, comprising:

a first current source for generating a second current according to the first current; and

a differential amplifier circuit for generating an output signal contained within a voltage range of the first power supply voltage and centered around the mid-point voltage to the internal circuit according to the second current.

2. The receiver circuit as claimed in claim 1, wherein the internal circuit comprises a plurality of transistors having a first gate oxide thickness.

3. The receiver circuit as claimed in claim 2, wherein the reference voltage circuit comprises a first PMOS transistor and a first NMOS transistor having the first gate oxide thickness.

4. The receiver circuit as claimed in claim 3, wherein the first PMOS transistor and the first NMOS transistor have a first p/n ratio.

5. The receiver circuit as claimed in claim 4, wherein the transistors of the internal circuit have the first p/n ratio.

6. The receiver circuit as claimed in claim 3, wherein the first PMOS transistor and the first NMOS transistor are connected in serial and between the first power supply voltage and ground, and the gates and the drains of the first PMOS transistor and the first NMOS transistor are connected.

7. The receiver circuit as claimed in claim 4, wherein the reference current circuit comprises:

a comparator circuit having a reverse input terminal, a non-reverse input terminal coupled to the gates of the first PMOS transistor and the first NMOS transistor, and an output terminal;

a first resistor coupled between the reverse input terminal and ground; and

a second current source coupled between the second power supply voltage and the first resistor for generating the first current flowing through the first resistor and generating the mid-point voltage at the connection point of the first resistor and the reverse input terminal.

8. The receiver circuit as claimed in claim 1, wherein the second current is referenced to the first current by a current mirror or equivalent circuitry.

9. The receiver circuit as claimed in claim 7, wherein the differential amplifier circuit comprises:

a second PMOS transistor having a first source coupled to the second current source, a first gate coupled to an I/O signal, and a first drain;

a third PMOS transistor having a second source coupled to the second current source, a second gate coupled to a reverse I/O signal, and a second drain;

a second resistor coupled between the connection point of the first drain and the internal circuit, and ground; and

a third resistor coupled between the connection point of the second drain and the internal circuit, and ground.

10. The receiver circuit as claimed in claim 7, wherein the second and third PMOS transistors have a second gate oxide thickness larger than the first gate oxide thickness.

11. The receiver circuit as claimed in claim 9, wherein the resistances of the second and third resistor are the same.

12. The receiver circuit as claimed in claim 1, wherein the mid-point voltage is approximately a switching point voltage of the internal circuit.

13. A receiver circuit, comprising:

an internal circuit supplied with a first power supply voltage and comprising a plurality of transistors having a first p/n ratio and a first gate oxide thickness;

a reference voltage circuit supplied with the first power supply voltage and comprising a first PMOS transistor and a first NMOS transistor having a first p/n ratio and the first gate oxide thickness, for outputting a reference voltage that is a mid-point voltage between the first power supply voltage and ground;

a reference current circuit for generating a first current according to the reference voltage; and

a receiving circuit supplied with a second power supply voltage higher than the first power supply voltage, comprising:

a first current source for generating a second current according to the first current; and

a differential amplifier circuit for generating an output signal contained within a voltage range of the first power supply voltage and centered around the mid-point voltage to the internal circuit according to the second current.

14. The receiver circuit as claimed in claim 13, wherein the first PMOS transistor and the first NMOS transistor are connected in serial and between the first power supply voltage and ground, and the gates and the drains of the first PMOS transistor and the first NMOS transistor are connected.

15. The receiver circuit as claimed in claim 13, wherein the reference current circuit comprises:

a comparator circuit having a reverse input terminal, a non-reverse input terminal coupled to the gates of

the first PMOS transistor and the first NMOS transistor, and an output terminal;

a first resistor coupled between the reverse input terminal and ground; and

a second current source coupled between the second power supply voltage and the first resistor for generating the first current flowing through the first resistor and generating the mid-point voltage at the connection point of the first resistor and the reverse input terminal.

16. The receiver circuit as claimed in claim 13, wherein the second current is referenced to the first current by a current mirror or equivalent circuitry.

17. The receiver circuit as claimed in claim 15, wherein the differential amplifier circuit comprises:

a second PMOS transistor having a first source coupled to the second current source, a first gate coupled to an I/O signal, and a first drain;

a third PMOS transistor having a second source coupled to the second current source, a second gate coupled to a reverse I/O signal, and a second drain;

a second resistor coupled between the connection point of the first drain and the internal circuit, and ground; and

a third resistor coupled between the connection point of the second drain and the internal circuit, and ground.

18. The receiver circuit as claimed in claim 17, wherein the second and third PMOS transistors have a second gate oxide thickness larger than the first gate oxide thickness.

19. The receiver circuit as claimed in claim 17, wherein the resistances of the second and third resistor are the same.

20. The receiver circuit as claimed in claim 13, wherein the mid-point voltage is approximately a switching point voltage of the internal circuit.